WHAT IS CLAIMED:

1. A circuit substrate associated with a signal-triggered digital circuit, the circuit substrate comprising:

a conducting interface for electrical connection to an input receiver, the input receiver receiving digital signals over said digital circuit and being responsive to triggering induced by said digital signals;

a conducting signal path, the conducting signal path being connected to said conducting interface, the signal path carrying said digital signals thereover; and

wherein the conducting interface is substantially rectangular in planar view and the conducting path connected thereto as aforesaid has a longitudinal centerline axis which forms an angle in a range of 110 to 160 degrees with respect to a side of the conducting interface to which the path is connected to thereby produce a reduced reflection of said digital signals at the connection between said conducting interface and said conducting path when compared to a connection wherein said angle has a value of 90 degrees.

2. The circuit substrate according to Claim 1, wherein the conducting signal path is connected to the conducting interface at a corner thereof.

3. The circuit substrate according to Claim 2, wherein the conducting signal path has a length which is at least 1/6th of a transition electrical length of the digital signal carried thereover, the transitional electrical length constituting a transient time of the said digital signal multiplied

by a propagation speed of the said digital signal over said conducting signal path, and wherein the transient time of the said digital signal is selected from the group comprising a rise time thereof and a fall time thereof.

4. The circuit substrate according to Claim 3, wherein the conducting signal path has a length which is at least said transition electrical length of the digital signal carried thereover.

5. The circuit substrate according to Claim 2, wherein said angle in a range of 110 to 160 degrees is an angle of 135 degrees.

6. The circuit substrate according to Claim 5, wherein the circuit substrate is a printed circuit board, the conducting interface is a pad and the conducting signal path is a trace.

7. The circuit substrate according to Claim 6, wherein the pad is substantially square in planar view and the trace has a width which is 1/5th of a width of a side of the pad to which the trace is connected.

8. The circuit substrate according to Claim 6, wherein when the input receiver is mounted to the pad, the trace has a thickness which is in a range of 1/5th to 1/6th of a thickness of the pad to which the trace is connected.

9. The circuit substrate according to Claim 6, wherein when the input receiver is mounted to the pad, the pad has a width of 22 mils and a thickness in a range of 6 mils to 7 mils, and wherein the trace has a width of 4 mils and a thickness of 1.2 mils.

10. The circuit substrate according to Claim 6, wherein the input receiver is comprised in a memory module and the trace carries digital signals in the form of control signals generated by a memory controller.

11. The circuit substrate according to Claim 10, wherein the memory module is a dual in-line memory module (DIMM) connected to the pad by a slot which accepts an edge connector of said module.

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